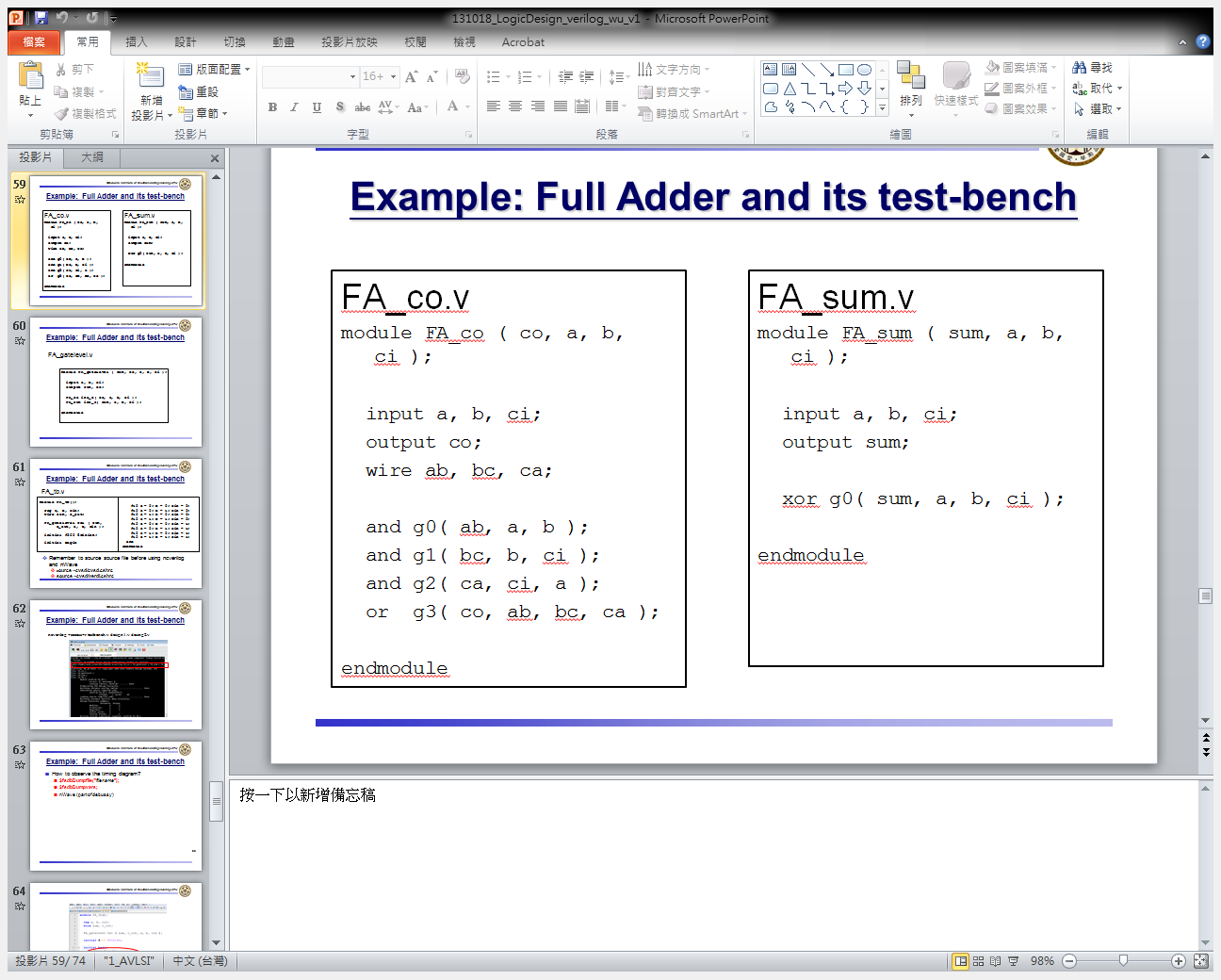
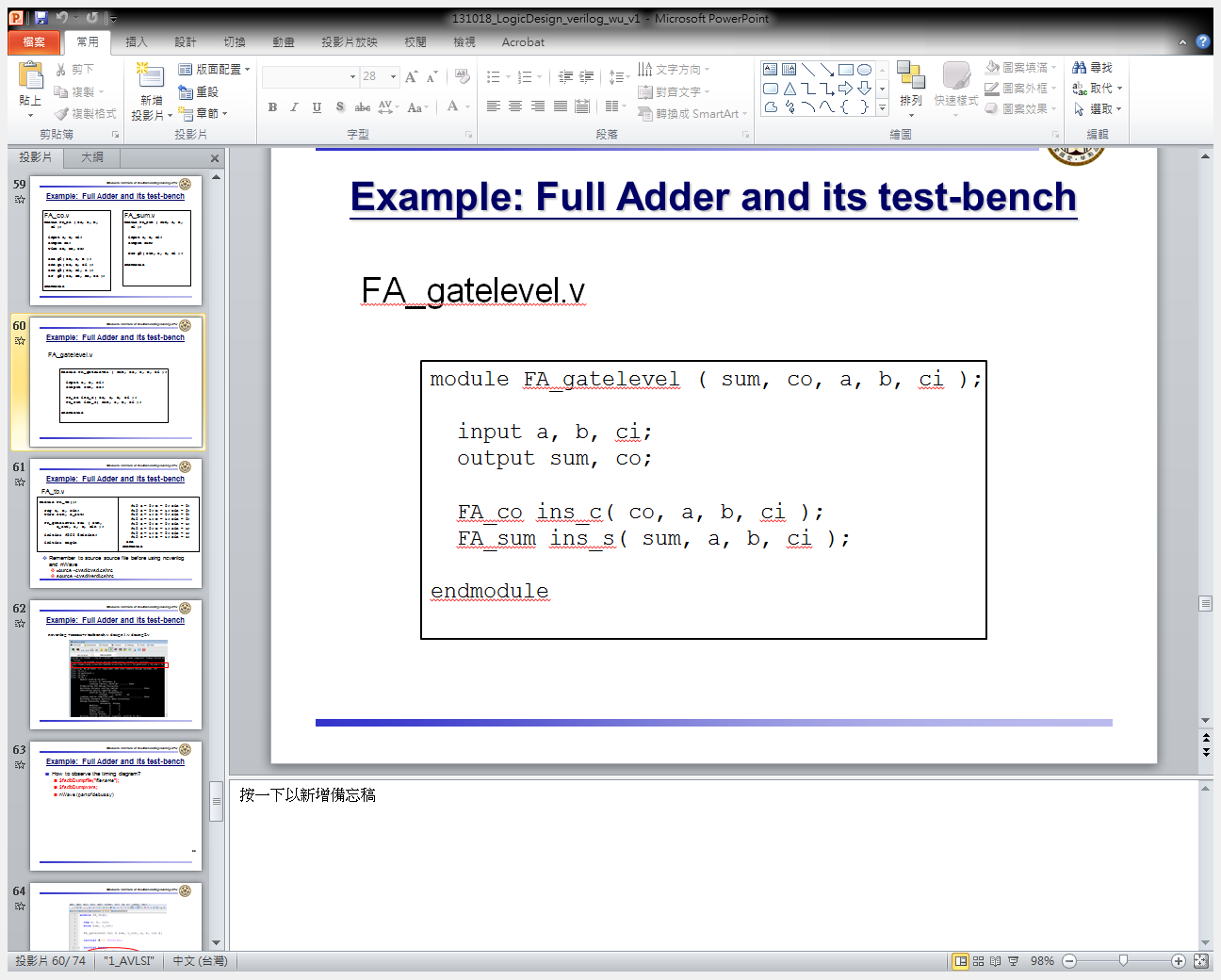
**Logic Design, Fall 2013**

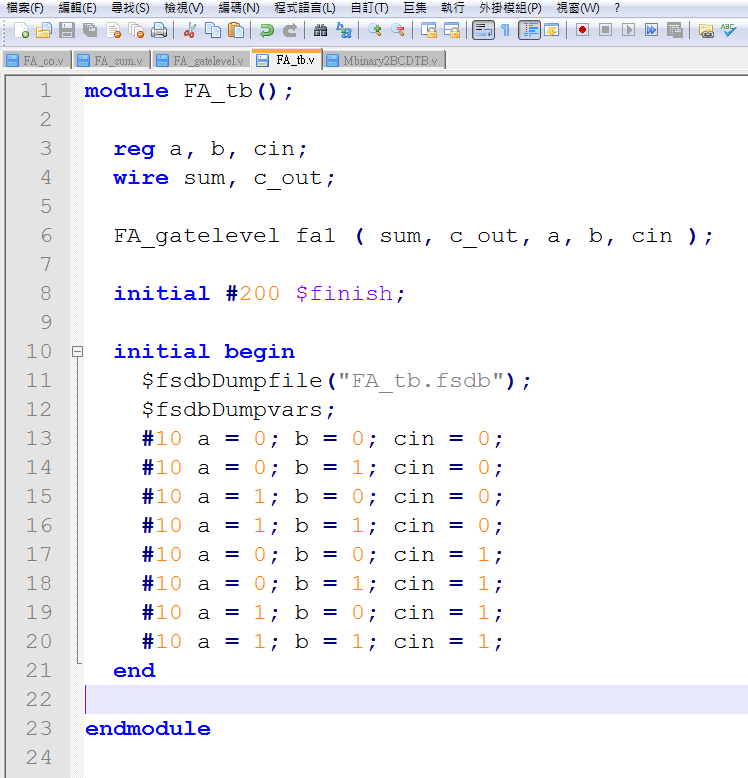
Verilog Lab1 – Full Adder

1. Finish FA\_co.v, FA\_sum.v, and FA\_gatelevel.v as p.31-p33 in slides.





1. Finish FA\_tb.v as p.64 in slides.



1. Source source.file before using ncverilog and nWave

* source /usr/cadence/cshrc
* source /usr/spring\_soft/CIC/verdi.cshrc

1. Simulate
   * ncverilog +access+r FA\_tb.v FA\_gatelevel.v FA\_sum.v FA\_co.v
2. Check result with wave
   * nWave &